



COMMERCIALIZATION ASSISTANCE PROGRAM

LAPACKrc™: High Performance Computing Linear Algebra Accelerator

Accelelogic

Business Opportunity:

Computational industries such as aerospace designs, weather forecasting, oil and gas exploration, rely on High Performance Computing (HPC) for simulations or data processing. An estimated 70% of HPC computations worldwide are spent solving large-scale linear equation systems. Accelelogic's technology can shift these intense computations from large vector or MPP computers to small dedicated linear-algebra solvers networked with super computers or even PCs. The HPC market is \$ 10 billion annually, and the segment associated with the Company's technology is estimated at \$7 billion.

Accelelogic is looking to develop its core business of providing a linear algebra co-processor (math kernel, application library and FPGA hardware) for accelerating linear-algebra problems. The company is interested in sponsored research to further develop application-specific kernels/solvers; government or commercial funding sources for specific end-use applications; licensees for integration with simulation and analysis software; strategic partnering arrangements with Value Added Resellers, accelerator manufacturers, or other solution providers; and licenses for integration into embedded signal processing applications, such as in radar signal processors, high-speed image processors, or proprietary HPC architectures.

Company Background:

Accelelogic is an R&D company specializing in the acceleration of linear algebra problems through radical algorithmic innovations and computational methods optimized with field-programmable gate arrays (FPGAs). This technology package brought to existence for the company a family of powerful "solvers" for entire classes of applications, creating mathematical libraries that reduce execution times from months, to hours, to seconds.

The company was founded in 2005 and currently has 12 employees. It is transitioning from sponsored research and development of high-performance linear algebra software library, to software application acceleration services and hardware/system/ASP solutions.

Industry Problem:

In certain industries simulation is a crucial function for remaining technologically competitive. The removal of bottlenecks is often a primary objective and computational

acceleration a necessary requirement. These companies compete on scientific discoveries and reduced time-to-market, supported by simulation and High Performance Computing (HPC), but often limited by long processing time, significant cost, and equipment size.

Technology:

Accellogic's core technology is a linear algebra co-processor, consisting of three primary components: 1) "on-the-fly" adaptively optimized linear-algebra solver; 2) FPGA based hardware accelerator; and 3) libraries that enable seamless acceleration of user's existing application code. Of particular note is its "on-the-fly" adaptively optimized linear-algebra solver, which is based on Accellogic's Bit Length Adaptive Space Time (BLAST) technology. It adjusts the computing architecture to the linear equation being solved for maintaining computational resolution while maximizing parallelism and speed.

Advantages:

- *Broad Applicability* – The LAPACKrc™ kernel addresses the general class of linear algebra, permitting diverse applications.
- *Ease of integration* – The LAPACKrc™ allows the acceleration existing codes (simulations or data processing) with just the addition of hardware accelerator and software libraries.
- *Portability* – The LAPACKrc™ FPGA-core can be rapidly moved to new FPGAs to enable quick integration with a signal processor to leverage larger, faster FPGAs with no rework.
- *Vendor Agnostic* – Any host card with a FPGA from any vendor can host the accelerator kernel, unlike GPU solutions.

Differentiating Feature:

Computational speed – Accellogic's technology can solve large-scale linear numerical computing at speeds 10x to 1000x faster than traditional HPC CPUs, because of its ability to adjust computing architecture to the linear equation through the BLAST component of its technology.

Stage of Development:

Proof of concept, feasibility, and initial prototyping of the LAPACKrc™ embedded FPGA code base and application linking software libraries have been completed. The initial prototypes have been delivered to government customers for testing with a variety of algebra solvers on HPC platforms. Accellogic has demonstrated a 10 times performance improvement as part of government partnerships using benchmarks based on real computationally intensive problems. Accellogic is currently developing application specific drivers, modifications, generalizations, and implementing additional algorithmic innovations under several SBIR Phase IIs.

Competing Technologies:

The major cost competitive solutions to the problem of effectively improving computation speeds are the following:

- *Multi-core CPUs* – Just as desktops are starting to enjoy the benefits of 2 or 4 processing cores within each CPU, so to are HPC machines starting to see hundreds of cores being deployed. However, they require more power, space and support equipment than dedicated processors (like FPGAs and GPUs).
- *Multi-machine Clusters* – The cores are physically separated by larger distances, but this solution is a way to utilize idle cycles of processors to get HPC processing speeds.

- *GPU supported CPUs* – This solution leverages the parallel processing capability of graphics processing chips to off-load math processing from the CPU but does not optimize linear algebra computations.
- *Math Accelerators* – FPGAs are combined with computational math software. As examples, HP and Nallatech have developed such firmware.

Applications:

The applications of Accelogic’s technology can be classified into four groups:

- *Development of Higher Performance Computers* – Embedding Accelogic’s technology into design of HPCs, as an added feature for specialized computation.
- *Development of Specialized Accelerators* – Integration of Accelogic’s technology with accelerator technology for device attachment to PCs or networked PCs.
- *Integration into Signal Processing Hardware* – Inclusion of Accelogic’s technology into embedded digital signal processing function for radars, missile seekers, and digital cameras.
- *Acceleration of Simulation and Data Processing Software* – Infusion of Accelogic’s technology to increase the speed of linear computations for weather forecasting, computation fluid dynamics, weapons simulation, and other Finite Element or Regression Analyses.

Benefits:

HPC Consumer (scientist, design engineer, analysts):

- Reduced time-to-solution of large and long running problems.
- Science and engineering breakthroughs from entirely new class of problem/solutions previously unreachable and addressed only by experimentation.
- Access to HPC computing at the desktop.

HPC Manufacturers & Software Sellers:

- Reduced cost of hardware with option from CPU to ancillary device.
- Reduce processing cost per computer cycle.
- New market segments to new computational users.

Companies and Organizations:

- Reduced costs to R&D, equipment, processing cycle, test-to-destruction experiments.

Intellectual Property:

Accelogic has sixteen patents in process, covering the major innovations behind the LAPACKrc™ library umbrella and also the FPGA architecture adjustment for linear equation categories.